What is claimed is:

1. A thyristor comprising:

a thyristor body region having a first base region coupled via a junction to a first emitter region that has a lightly-doped portion extending along and adjacent to the junction, the lightly-doped portion having a significantly lighter dopant concentration, relative to the dopant concentration of the first base region; and

a thyristor control port configured and arranged for capacitively coupling at least to the second base region for controlling current flow in the thyristor body region.

2. The thyristor of claim 1, wherein the thyristor body region includes a plurality of contiguous regions of opposite polarity including the first base and emitter regions and a second base region coupled to a second emitter region, the first and second base regions being coupled to one another.

3. The thyristor of claim 2, wherein a heavily-doped portion of the first emitter region is coupled to a reference voltage line and wherein the lightly-doped portion of the first emitter region is immediately adjacent to the first base region.

4. The thyristor of claim 3, wherein the second emitter region is electrically coupled to a bit line via a switch and wherein the relative dopant concentration of the first emitter region is adapted for data storage and manipulation at the second emitter region,

responsive to signals applied at the reference voltage line, the control port and the bit line.

5. The thyristor of claim 1, wherein the thyristor body region is disposed on a buried insulator layer.

6. The thyristor of claim 1, wherein the first base region and the first emitter region have similar active doping levels.

7. The thyristor of claim 6, wherein the lightly-doped portion of the first emitter region is configured and arranged for preventing overlap of the first base region and a more heavily-doped portion of the first emitter region.

8. A thyristor-based semiconductor device including a thyristor electrically coupled in series with a pass device, the thyristor-based semiconductor device comprising:

a thyristor body region having a first base region coupled to a first emitter region via a junction and a second base region coupled to a second emitter region, the first and second base regions being coupled to one another, the first emitter region having a heavily doped portion and a lightly-doped portion, the lightly-doped portion extending along and adjacent to the junction and having a significantly lighter dopant concentration, relative to the dopant concentration of the first base region; and

a thyristor control port configured and arranged for capacitively coupling a signal to the second base region via a dielectric material disposed between the thyristor control port and the second base region; and

a pass device electrically coupled to the second emitter region and configured and arranged for controlling current flow to and from the first emitter region.

9. The thyristor-based semiconductor device of claim 8, wherein the lightly-doped portion of the first emitter region is doped to a concentration that is about $1/10^{th}$ of the dopant concentration of the first base region.

10. The thyristor-based semiconductor device of claim 8, wherein the heavily-doped portion of the first emitter region is doped to a concentration of about 5 times greater than the dopant concentration of the first base region.

11. The thyristor-based semiconductor device of claim 8, wherein the thyristor is a thin capacitively-coupled thyristor.

12. The thyristor-based semiconductor device of claim 11, wherein the control port and the second base region are configured and arranged such that a signal applied to the control port changes the potential across a majority of a cross-section of the second base region.

13. The thyristor-based semiconductor device of claim 8, wherein the thyristor and control port are configured and arranged outflowing minority carriers from the second base region in response to a voltage pulse being applied to the control port.

14. The thyristor-based semiconductor device of claim 8, wherein the thyristor body region is disposed on a buried insulator layer.

15. The thyristor-based semiconductor device of claim 8, wherein the second emitter region is electrically coupled to the pass device.

16. The thyristor-based semiconductor device of claim 15, wherein the second emitter region is configured and arranged for storing data and wherein the pass device is configured and arranged to provide access to the data.

17. The thyristor-based semiconductor device of claim 16, wherein the pass device includes a transistor having a first and second source/drain region separated by a channel region and with a gate over the channel region, the first source/drain region being electrically coupled to the second emitter region and the second source/drain region being electrically coupled to a bit line, the gate being configured and arranged for controlling current flow between the bit line and the second emitter region.

18. The thyristor-based semiconductor device of claim 8, further comprising a plurality of memory cells over the buried insulator region, one of the cells including the

thyristor-based semiconductor device of claim 5, each cell having a thyristor electrically coupled in series with a pass device, wherein said heavily-doped emitter region is shared with a thyristor in an adjacent memory cell.

19. The thyristor-based semiconductor device of claim 8, further comprising a second thyristor control port configured and arranged to capacitively couple a signal to the first base region via a dielectric material disposed between the second thyristor control port and the first base region.

20. The thyristor-based semiconductor device of claim 19, wherein the second thyristor control port is configured and arranged for masking a portion of the first emitter region during implantation.

21. The thyristor-based semiconductor device of claim 20, wherein the second thyristor control port is adapted to mask the lightly-doped portion of the first emitter region.

22. The thyristor-based semiconductor device of claim 8, wherein the lightly-doped portion of the first emitter region has a dopant concentration that is on the same order as the second base region.

23. The thyristor-based semiconductor device of claim 8, wherein the heavily-doped portion of the first emitter region has a dopant concentration that is on the same order as the second base region.

24. The thyristor of claim 23, wherein the lightly-doped portion of the first emitter region is configured and arranged for preventing overlap of the first base region and the heavily-doped portion of the first emitter region.

25. A method for manufacturing a thyristor-based semiconductor device, the method comprising:

forming a thyristor having a body region in a substrate with a plurality of contiguous regions of opposite polarity including a first base region coupled to a first emitter region via a junction and a second base region coupled to a second emitter region, the first and second base regions being coupled to one another, wherein the first emitter region is formed by doping a lightly-doped portion with a significantly lighter dopant concentration than the dopant concentration of the first base region and doping a heavily-doped portion, the lightly-doped portion extending along and adjacent to the junction; and

forming a thyristor control port configured and arranged for capacitively coupling at least to the second base region for controlling current flow in the thyristor body region.

26. The method of claim 25, further comprising forming a mask over the lightly-doped portion, wherein doping the heavily-doped portion includes using the mask to mask the lightly-doped portion.

27. The method of claim 26, wherein forming the mask includes forming a word line to mask the lightly-doped portion.

28. The method of claim 25, wherein forming a thyristor control port includes forming a word line having a spacer on a sidewall thereof, wherein forming the thyristor includes using the spacer to mask a portion of the substrate during doping of the first base region.

29. The method of claim 28, wherein forming the thyristor includes using an angled implant to form the first base region.

30. The method of claim 25, wherein forming a heavily-doped portion of the emitter region includes doping the heavily-doped portion with a significantly higher dopant concentration than the dopant concentration of the first base region.

31. The method of claim 25, wherein forming a thyristor includes doping the heavily-doped portion of the first emitter region and the first base region to a similar dopant concentration.

32. The method of claim 31, further comprising using the lightly-doped portion of the first emitter region to prevent overlap of the heavily-doped portion of the first emitter region and the first base region.